This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the substrate being rotated during the formation of semiconductor layer, the semiconductor layer including at least two elements distributed to define an initial compositional variation within the semiconductor layer; and

annealing the semiconductor layer to reduce the initial compositional variation throughout the semiconductor layer by diffusing at least one of the at least two elements throughout the semiconductor layer,

wherein the initial compositional variation is caused by the rotation of the substrate during the formation of the semiconductor layer.

2. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements distributed to define an initial compositional variation within the semiconductor layer; and

annealing the semiconductor layer to reduce the initial compositional variation throughout the semiconductor layer by diffusing at least one of the at least two elements throughout the semiconductor layer,

wherein the substrate has a first lattice constant, the semiconductor layer has a second lattice constant, and the first lattice constant differs from the second lattice constant.

3. – 15. (Cancelled)

16. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements distributed to define an initial compositional variation within the semiconductor layer; and

annealing the semiconductor layer to reduce the initial compositional variation throughout the semiconductor layer by diffusing at least one of the at least two elements throughout the semiconductor layer,

wherein the semiconductor layer is annealed at an annealing temperature greater than the deposition temperature.

17. – 25. (Cancelled)

26. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements distributed to define an initial compositional variation within the semiconductor layer; and

annealing the semiconductor layer to reduce the initial compositional variation throughout the semiconductor layer by diffusing at least one of the at least two elements throughout the semiconductor layer,

wherein one of the at least two elements comprises germanium and the top surface of the semiconductor layer is planarized after the semiconductor layer is annealed.

27. – 30. (Cancelled)

31. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements distributed to define an initial compositional variation within the semiconductor layer;

annealing the semiconductor layer to reduce the initial compositional variation throughout the semiconductor layer by diffusing at least one of the at least two elements throughout the semiconductor layer;

planarizing a top surface of the semiconductor layer;

bonding a top surface of the semiconductor layer to a wafer; and

removing at least a portion of the substrate,

wherein at least a portion of the semiconductor layer remains bonded to the wafer after the portion of the substrate is removed.

32. – 34. (Cancelled)

35. (Previously presented) A method for forming a semiconductor substrate, the method comprising:

providing a substrate;

forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements, the elements being distributed to define an initial compositional variation within the semiconductor layer;

annealing the semiconductor layer to reduce the initial compositional variation;

planarizing a top surface of the semiconductor layer;

forming a second layer over the semiconductor layer subsequent to planarizing the top surface of the semiconductor layer;

bonding a top surface of the second layer to a wafer; and

removing at least a portion of the substrate,

wherein at least a portion of the second layer remains bonded to the wafer after the portion of the substrate is removed.

36. – 44. (Cancelled)

45. (Previously presented) A method for forming a semiconductor structure, the method comprising:

providing a substrate;

selecting a first plurality of parameters suitable for forming a semiconductor layer over a top surface of the substrate, the semiconductor layer including at least two elements, the elements being distributed to define a compositional variation within the semiconductor layer;

forming the semiconductor layer having a haze; and

planarizing the semiconductor layer to remove the haze,

wherein the haze comprises a fine-scale roughness wavelength of <1 micrometer.

46. (Original) The method of claim 45 wherein forming the semiconductor layer comprises forming a lower portion including a superlattice and forming an upper portion over the lower portion, the upper portion being substantially free of a superlattice.

47. (Original) The method of claim 45 wherein the first plurality of parameters comprises at least one parameter selected from the group consisting of temperature, precursor, growth rate, and pressure.

48. (Original) The method of claim 45, further comprising:

cleaning the semiconductor layer after planarizing,

wherein the semiconductor layer remains substantially haze-free after cleaning.

49. (Original) The method of claim 45, further comprising:

selecting a second plurality of parameters suitable for forming a substantially haze-free regrowth layer over the semiconductor layer, the semiconductor layer including at least two elements, the elements being distributed to define a compositional variation within the semiconductor layer; and

forming the substantially haze-free regrowth layer.

50. (Original) The method of claim 49 wherein the first plurality of parameters comprises a first temperature, the second plurality of parameters comprises a second temperature, and the first temperature is higher than the second temperature.

51. (Original) The method of claim 49 wherein the first plurality of parameters comprises a first growth rate, the second plurality of parameters comprises a second growth rate, and the first growth rate is higher than the second growth rate.

52. (Original) The method of claim 49 wherein forming the regrowth layer comprises forming a lower portion including a superlattice and forming an upper portion over the lower portion, the upper portion being substantially free of a superlattice.

53. – 79. (Cancelled)

80. (Previously presented) The method of claim 45, wherein after planarization, a top surface of the semiconductor layer has a roughness root-mean-square of less than 5 angstroms in a scan area of 40 $\mu m \times 40\ \mu m$.

81. (Previously presented) The method of claim 80, wherein after planarization, the semiconductor layer top surface has a roughness root-mean-square of less than 1 angstrom in a scan area of 40 $\mu m \times 40\ \mu m$.

82. (New) The method of claim 35 wherein the top surface of the semiconductor layer is planarized before the semiconductor layer is annealed.

83. (New) The method of claim 35 wherein the top surface of the semiconductor layer is planarized while the semiconductor layer is annealed.

84. (New) The method of claim 35 wherein the top surface of the semiconductor layer is planarized after the semiconductor layer is annealed.

85. (New) The method of claim 35 wherein planarizing comprises at least one of chemical-mechanical polishing, plasma planarization, wet chemical etching, gas-phase chemical etching, oxidation followed by stripping, or cluster ion beam planarization.

86. (New) The method of claim 85 wherein chemical-mechanical polishing comprises a first and a second step and the semiconductor layer is annealed between the first and the second chemical-mechanical polishing steps.

87. (New) The method of claim 85 wherein chemical-mechanical polishing comprises a first and a second step and the semiconductor layer is annealed before the first chemical-mechanical polishing step.

88. (New) The method of claim 85 wherein planarizing comprises a high temperature step and the semiconductor layer is annealed during the high temperature planarization step.

89. (New) The method of claim 35 wherein the second layer comprises a material having a lattice constant substantially equal to a lattice constant of the semiconductor layer.

90. (New) The method of claim 35 wherein the second layer comprises a material having a lattice constant substantially different from a lattice constant of the semiconductor layer.

91. (New) The method of claim 35 wherein the second layer comprises (i) a lower portion having a superlattice and (ii) an upper portion disposed over the lower portion, the upper portion being substantially free of a superlattice.

92. (New) The method of claim 35, further comprising:

forming a relaxed graded layer over the substrate,

wherein the semiconductor layer is formed over the relaxed graded layer.

93. (New) The method of claim 35, further comprising:

forming a protective layer over the semiconductor layer prior to annealing the semiconductor layer.

94. (New) The method of claim 93 wherein the protective layer comprises a material that is substantially inert with respect to the semiconductor layer.

95. (New) The method of claim 94 wherein the protective layer is selected from the group consisting of silicon dioxide, silicon nitride, and combinations thereof.

96. (New) The method of claim 35 wherein the substrate has a first lattice constant, the semiconductor layer has a second lattice constant, and the first lattice constant differs from the second lattice constant.

97. (New) The method of claim 35 wherein a first element has a first concentration, a second element has a second concentration, and each of the first and second concentrations is at least 5%.

98. (New) The method of claim 35 wherein the initial compositional variation varies periodically within the semiconductor layer in a direction perpendicular to a semiconductor layer deposition direction.

99. (New) The method of claim 98 wherein the compositional variation defines a column within the semiconductor layer, the column having a width and a period.

100. (New) The method of claim 99 wherein the columnar period is less than approximately 2000 nanometers.

101. (New) The method of claim 100 wherein the columnar period is less than approximately 1000 nanometers.

102. (New) The method of claim 99 wherein the semiconductor layer is annealed at an annealing temperature sufficient to diffuse at least one of the two elements through a diffusion length at least equal to a quarter of the columnar period.

103. (New) The method of claim 99 wherein the semiconductor layer is annealed for a duration sufficient to diffuse at least one of the two elements through a diffusion length at least equal to a quarter of the columnar period.

104. (New) The method of claim 35 wherein the initial compositional variation varies in a direction parallel to a semiconductor layer deposition direction and defines a superlattice having a periodicity.

105. (New) The method of claim 104 wherein the superlattice periodicity is less than approximately 100 nanometers.

106. (New) The method of claim 105 wherein the superlattice periodicity is less than approximately 50 nanometers.

107. (New) The method of claim 106 wherein the superlattice periodicity is less than approximately 10 nanometers.

108. (New) The method of claim 104 wherein the semiconductor layer is annealed at an annealing temperature sufficient to diffuse at least one of the two elements through a diffusion length at least equal to a quarter-period of the superlattice.

109. (New) The method of claim 104 wherein the semiconductor layer is annealed for a duration sufficient to diffuse at least one of the two elements through a diffusion length at least equal to a quarter-period of the superlattice.

110. (New) The method of claim 35 wherein the semiconductor layer is annealed at an annealing temperature greater than the deposition temperature.

111. (New) The method of claim 110 wherein the annealing temperature is greater than about 800 °C.

112. (New) The method of claim 111 wherein the annealing temperature is greater than about 1000 °C.

113. (New) The method of claim 110 wherein the semiconductor layer is annealed at an annealing temperature below a melting point of the semiconductor layer.

114. (New) The method of claim 113 wherein the annealing temperature is less than about 1270 °C.

115. (New) The method of claim 35 wherein one of the at least two elements comprises silicon.

116. (New) The method of claim 35 wherein one of the at least two elements comprises germanium.

117. (New) The method of claim 35 wherein the semiconductor layer is formed in a horizontal flow deposition reactor.

118. (New) The method of claim 35 wherein the rotation of the substrate results in higher fraction of a first element the semiconductor layer disposed in a leading edge of the substrate.

119. (New) The method of claim 35 wherein the layer is formed in a single wafer reactor.

120. (New) The method of claim 35 wherein the wafer comprises an insulating layer.

121. (New) The method of claim 45 wherein planarizing comprises at least one of chemical-mechanical polishing, plasma planarization, wet chemical etching, gas-phase chemical etching, oxidation followed by stripping, or cluster ion beam planarization.

122. (New) The method of claim 45 wherein one of the at least two elements comprises silicon.

123. (New) The method of claim 45 wherein one of the at least two elements comprises germanium.